

S/Unknown

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Anthony N. DeFazio et al.	Examiner:	Unknown
Serial No.:	Unknown	Group Art Unit:	Unknown
Filed:	N/A	Docket No:	H0004594 (256.173US1)
Title:	IN-RUSH CURRENT MANAGEMENT		

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PRELIMINARY AMENDMENT

MS Patent Application  
Commissioner for Patents  
P.O.Box 1450  
Alexandria, VA 22313-1450

Before taking up the above-identified application for examination, please enter the following amendments.

IN THE DRAWINGS

Corrected Formal Drawings are supplied herewith.

In FIG. 1, Box 135, "STIMULATION" has been changed to "SIMULATION".

IN THE SPECIFICATION

**[00015]** A clock synthesis function 120 of the power conversion device is coupled to the power converter ~~115~~ 110 and provides for manipulation of clock attributes of the power converter ~~115~~ 110, including duty cycle and frequency. In one embodiment, this function is provided by a field programmable gate array (FPGA), but could be any re-programmable logic device. The device has non-volatile memory on board, and is also reprogrammable via an external connector in one embodiment. Load 115 may be one or more of load types, including linear and non-linear. In one embodiment, the load comprises a ring laser gyro including gas plasma elements. Such a load requires a high voltage for a short period of time. For some such loads, 2500 to 3000 volts is required for a short period of time. This resulted in large in-rush currents in prior devices. This in-rush current is measured in one embodiment by a circuit 125. In one embodiment, a resistive shunt or inductive current probe with a wide bandwidth oscilloscope is used to measure the in-rush current. Other methods may also be employed to observe the transient turn on characteristics, such as current divided by power versus time.

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Assignee: Intel Corporation

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Dkt: 256.173US1 (INTEL)

The Examiner is invited to contact the below-signed attorney with any questions regarding the present application.

Respectfully Submitted,

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This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to The Commissioner for Patents, Mail Stop Patent Application, P.O. Box 1450, Alexandria, VA 22313-1450.